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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/519,877	02/17/2006	Ichiro Hase	09792909-6063	7426
26263 7590 10/17/2007 SONNENSCHN NATH & ROSENTHAL LLP P.O. BOX 061080 WACKER DRIVE STATION, SEARS TOWER CHICAGO, IL 60606-1080			EXAMINER PATTON, PAUL E	
			ART UNIT 2822	PAPER NUMBER
			MAIL DATE 10/17/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/519,877	Applicant(s) HASE, ICHIRO	
	Examiner Paul E. Patton	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 February 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,5,6,12,17 and 18 is/are rejected.
- 7) ☐ Claim(s) 3,4,7-11 and 13-16 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 February 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some c) ☒ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>12/30/2004</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 5,6,12,17 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Hase et al., (USPAT 6,365,925 B2) Hase.

3. As to claim 1, Hase discloses and shows (Fig 12) a semiconductor device having a source electrode 17a), a drain electrode (17b), a gate electrode (20) disposed between the source electrode and the drain electrode, and a channel layer (14) composed of a semiconductor which serves as a current path between the source electrode and the drain electrode, characterized by comprising: a first barrier layer (115) composed of a semiconductor having a p-type conductive region doped with a p-type impurity of high concentration under the gate, a second barrier layer (13) disposed on an opposite side of said first barrier layer while placing said channel layer in between and is composed of a semiconductor having an electron affinity smaller than that of said channel layer, and a third barrier layer (121) disposed between said first barrier layer and said channel layer and is composed of a semiconductor having an electron affinity smaller than that of said channel layer, wherein a relation below:

$$\chi_1 - \chi_3 \leq 0.5 * (E_{g3} - E_{g1}) \quad (1)$$

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is satisfied, where x_1 is electron affinity of said first barrier layer, E_{g1} is a band gap thereof, x_3 is electron affinity of said third barrier layer, and E_{g3} is a band gap thereof.

Note that due to the materials comprising layer 15b (GaAs) and 121a (AlGaAs) equation 1 is inherently satisfied. (Column 4, lines 22-68 & column 8, line 51—column 9, line 5).

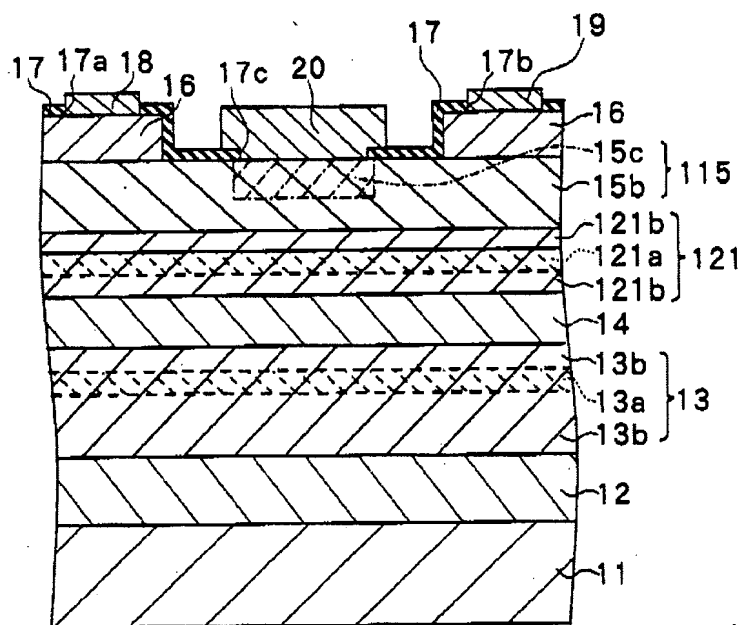


FIG.12

4. As to claim 2, Hase discloses the third barrier layer (121) is composed of a III-V compound semiconductor containing at least any one of Ga, Al and In as a Group III element, and containing at least either one of As and P as a Group V element. (Column 8, lines 51-59).

5. As to claim 5, Hase discloses that the thickness of said third barrier layer is 20 nm or less. (Column 8, lines 60-65).

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6. As to claim 6, Hase discloses that the first barrier layer is GaAs. (Column 5, lines 10—13).

7. As to claim 12, Hase discloses that the p-type impurity doped to said first barrier layer is Zn. (Column 5, lines 47-49).

8. As to claim 17, Hase discloses that any one layer of the first barrier layer, third barrier layer, fourth barrier layer and sixth barrier layer is doped with n-type impurity of high concentration. (Column 8, lines 59-63).

9. As to claim 18, Hase discloses that the semiconductor composing the channel layer (14) is InGaAs or GaAs. (Column 7, lines 29-32)

Allowable Subject Matter

10. Claims 3,4,7 – 11, and 13 – 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record taken alone or in combination fails to anticipate or render obvious, as shown in claim 3, the third barrier layer is InGaP or AlGaInP or InGaAsP, and as shown in claim 4, that the third barrier layer has an alloy with an Al composition ratio of 50% or more, as shown in claim 7 a fourth barrier layer with an electron affinity less than the channel layer, as shown in claim 8 a fourth barrier layer comprised of AlGaAs or GaAs; as shown in claim 9 the sum of the thicknesses of the third and forth barrier layers in 20 nm or less; as shown in claim 10 a fifth barrier layer; as shown in claim 11 a fifth barrier layer comprising GaAs; as shown in claim 13, a sixth barrier

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layer; as shown in claim 14 the sixth barrier layer composed of GaAs or AlGaAs; as shown in claim 15 the sum of the thickness of the third and sixth barrier layers is 25 nm or less; and as shown in claim 16 as semiconductor layer on the gate electrode side containing one-tenth or less impurity as compared with a maximum impurity concentration of the p-type impurity contained in the first barrier layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E. Patton whose telephone number is 571-272-9762. The examiner can normally be reached on 7:00 - 5:30 Monday through Thursday.

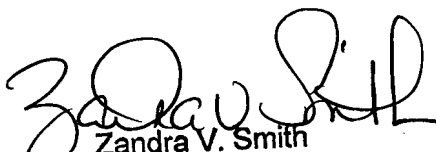
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


PEP

Paul E Patton
Examiner
Art Unit 2822


Zandra V. Smith
Supervisory Patent Examiner
12 Oct 2007